## REMARKS

The above amendments and following remarks attend to each and every rejection and objection presented in the pending March 23, 2005 office action. Claims 1-38 remain pending, with claims 1, 12 and 24 being independent.

## SPECIFICATION

The paragraph spanning lines 19-26 on page 7 of the specification is amended to correct two typographical errors related to figure numbering. This paragraph corresponds to ¶[0034] on page 3 of U.S. Application Publication No. 20040266179. No new matter is added with this amendment.

## CLAIM REJECTIONS – 35 U.S.C. §102

Claims 1, 3, 4, 6-15, 17, 18, 22-24, 26, 27, 30-33, 35, 37 and 38 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,106,461 granted to Volfson et al. (hereinafter "Volfson"). Respectfully, we disagree.

To anticipate a claim, Volfson must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989).

Volfson does not teach every element of claims 1, 3, 4, 6-15, 17, 18, 22-24, 26, 27, 30-33, 35, 37 and 38. Applicant respectfully submits that many differences exist in the claimed elements between Volfson and applicant's claimed invention such that Volfson cannot be said to anticipate applicant's invention. More specifically, Volfson does not teach every element of applicant's claims 1, 3, 4, 6-15, 17, 18, 22-24, 26, 27, 30-33, 35, 37 and 38, as demonstrated herein below.

A brief summary of the instant application versus Volfson's technology may be helpful before specific discussion of the claims. In summary, applicant teaches a process for patterning self-aligned via contacts. The via contacts are self-aligned since they are formed from the same photoresist pattern used to etch the underlying junction stack. A dielectric layer is deposited upon the etched edges of junction stacks and the patterned photoresist used to etch the junction stacks such that, when the dielectric coated photoresist caps are removed by directional ion milling, for example, resulting via contact pads are aligned with the junction stacks. As shown in FIG. 6B, the direction of ion stream 602 is substantially parallel to the plane of wafer 302 such that only coated caps 512, 608, 610 are milled away to achieve the self aligned via contacts 514, 614. Independent claims 1, 12 and 24 each specifically recite, "ion etching at a low angle."

On the other hand, Volfson discloses a process whereby vias are electroplated into etched holes. The patterned photoresist is not used to form junction stacks. The patterned photoresist is used to etch vias to connect previously etched structures – thus the patterned photoresist lacks the preferred self-alignment property provided by applicant's disclosure.

In addition, Volfson discloses the use of reactive ion etching (RIE) to pattern an aluminum mask, thereby requiring the ion beam to be substantially perpendicular to the plane of the aluminum mask (and thereby the wafer).

To summarize, Volfson does not:

1 – disclose applicant's process of directional ion etching process,

2 – disclose that any photoresists are dielectrically coated,

3 – disclose that the ion beam is at a low angle (e.g., parallel) to the plane of the wafer,

4 – disclose that the low angle (e.g., parallel) ion beam is for removing the dielectric coated photoresist to form one or more self-aligned via contacts; or

5 – disclose that it is the removal of the coated photoresists that forms the one or more self-aligned via contacts.

**Claim 1**

Applicant's claim 1 recites a directional ion etching process for patterning self-aligned via contacts including:

depositing a photoresist on a patterned layer;

masking the photoresist to provide at least one protected area, the photoresist being developed to remove the photoresist from the non-protected area;

depositing a dielectric coating upon the patterned layer and the remaining photoresist; and

ion etching at a low angle relative to the patterned layer to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact.

The Examiner states that Volfson discloses the elements of claim 1. For example, the Examiner asserts that Volfson deposits a dielectric coating upon a patterned layer and remaining photoresist (pending Office Action, page 2, number 1). The Examiner cites FIG. 3E and reference number 216 in support of this position. Respectfully, applicant disagrees.

Volfson discloses a very different process from the directional ion etching recited in claim 1. Among other differences, applicant requires that a dielectric coating is deposited upon the patterned layer ***and the remaining photoresist***. Volfson does not deposit a dielectric coating upon a photoresist. Rather, in the process of Volfson, a layer of copper is "electroplated through the photoresist mask ***and the photoresist is removed***" (col. 7, lines 60-62, emphasis added). Volfson then applies "a layer 216 of polyimide about 20-25 microns thick is applied" (col. 8, lines 1-2).

Respectfully, Volfson does not, **and indeed *cannot***, deposit layer 216 onto the photoresist since, in the process of Volfson, this photoresist is removed after etching. Further, applicant requires ion etching at a low angle relative to the patterned layer to remove the dielectric coated photoresist. Nowhere does Volfson teach ion etching at a low angle, in fact, there is no mention of any etching angle within Volfson. Further, the ion etching that is discussed must be performed at a substantially vertical angle relative to the aluminum mask.

As Volfson does not deposit a dielectric coating upon a photoresist, Volfson also does not (and cannot) etch to remove a dielectric coated photoresist.

Reconsideration of claim 1 is respectfully requested.

**Claims 3, 4 and 6-11:**

Claims 3, 4 and 6-11 depend from claim 1 and benefit from like argument. As such, applicant includes herein by reference each and every statement made above. In addition, these claims include further features that patentably distinguish over Volfson.

For example, claim 3 requires that "the ion etching is accomplished by a physically assisted process." Claim 4 requires that "the physically assisted process is reactive ion etching." As noted above with respect to claim 1, the etching is performed at a low angle relative to the patterned layer. Volfson teaches neither a physically assisted ion etching performed at a low angle (claim 3), nor reactive ion etching performed at a low angle (claim 4).

Claim 6 requires etching the patterned layer ***following the developing of the photoresist*** and prior to the depositing of the dielectric coating. As noted above with respect to claim 1, applicant etches the patterned layer to remove the dielectric coated photoresist. First, there is no dielectric coated photoresist in Volfson. Second, Volfson first etches to remove titanium and copper, ***then*** removes the photoresist, then etches again ***after photoresist has been removed***:

> "A layer of photoresist 208 of about 1-1.5 .mu. is applied on top of the titanium 206. See FIG. 3A. Next, the photoresist 208 is patterned...The titanium and the copper are then etched away in the defined areas and the photoresist is removed" (col. 7, lines 42-48).

Claim 7 requires that the protected area be the intended location of at least one self-aligned via contact. Volfson recites that "using the aluminum as a mask, the polyimide is etched to open holes for vias." See Volfson col. 8, lines 7-8. This process clearly differs from that of claim 7. For example, since the polyimide is etched using the aluminum mask to open holes for vias, the protected areas cannot be the intended location of the vias. The protected areas of Volfson should in fact be described as the opposite of Volfson's intended location of the vias.

Claim 8 recites that "the dielectric coated photoresists extend substantially perpendicularly from the surface of the patterned layer, such that the low angle of ion etching relative to the patterned layer is a high angle relative to the extending coated photoresists." As noted, Volfson does not teach a dielectric coated photoresist, let alone a dielectric coated photoresist extending substantially perpendicular from the surface of the patterned layer.

Claim 9 requires that the via contact exposed by ion etching be in substantially the same plane as the remaining dielectric. Volfson recites, "... copper vias 222A and 222B are then ***electroplated into*** the openings..." (col. 8 lines 14-15, emphasis added). The process of Volfson clearly requires an additional step to form vias and does not teach that via contacts are exposed by ion etching. Volfson also does not, therefore, teach a via contact that is exposed by ion etching and that is in substantially the same plane as the remaining dielectric.

Claim 10 recites "depositing an additional patterned layer and repeating the recited process to establish at least one additional self-aligned contact to the additional patterned layer." The Examiner cites reference numbers 224, 226 and 228 of figure 3F in Volfson as representing deposition of additional patterned layers to establish at least one additional self aligned contact to the additional patterned layer. Applicant respectfully notes that Volfson's process is still clearly different from that required by claim 10.

Volfson does not and can not teach the process of applicant's claim 1; thus, logically, Volfson does not and can not teach repeating applicant's process. For example, the "layers of chromium, copper and titanium, respectively labeled 224, 226 and 228 are successively deposited, for example by sputtering" (col. 8 lines 19-21). Volfson continues, "as for the previous via layer, the vias in the polyimide are etched using the aluminum mask ... using the first copper layer 204 as an electrode, copper vias 236 and 238 are electroplated" (col. 8, lines 38-43). Again, the process of Volfson is clearly different from that required by claim 10.

Claim 11 depends from claim 10, and so benefits from like argument, included herein by reference.

Reconsideration of claims 3, 4 and 6 through 11 is respectfully requested.

**Claim 12:**

Claim 12 recites a directional ion etching process for patterning self-aligned via contacts, including:

depositing a first conductive layer on a wafer substrate;

depositing a junction layer upon the first conductive layer, the junction layer being in electrical contact with the first conductive layer;

depositing a photoresist upon the junction layer;

masking the photoresist to provide a plurality of junction stacks, the photoresist being developed and the exposed junction layer being etched;

depositing a dielectric coating upon the etching exposed surfaces and the photoresist; and

ion etching at a low angle relative to the wafer substrate to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact.

Again, Volfson does not disclose depositing a dielectric coating upon the etching exposed surfaces of junction stacks ***and the photoresist***, as required in claim 12. Further, Volfson does not disclose ***ion etching at a low angle*** relative to the wafer substrate to remove the dielectric coated photoresist to provide at least one self aligned via contact, as in claim 12. As argued above, since the photoresist used to etch the junction stacks (and the etched surfaces of the junction stacks) is coated with a dielectric, when the dielectric coated photoresist 'caps' are removed by directional ion milling, a self-aligned via contact results. Volfson does not describe such a process and therefore cannot anticipate claim 12.

Reconsideration of claim 12 is respectfully requested.

**Claims 13-15, 17, 18, 22 and 23:**

Claims 13-15, 17, 18, 22 and 23 depend from claim 12 and benefit from like argument. As such, applicant includes herein by reference each and every statement made with respect to claim 12, above. In addition, these claims have additional features that patentably distinguish from Volfson. For example:

Claim 13 further recites:

depositing a first photoresist layer on the first conductive layer;

masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows; and

depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows before the junction layer is deposited.

As previously noted, Volfson fails to teach at least two elements of claim 12. The additional elements of claim 13 are thus part of a process that is different from the process of Volfson. Claim 13 is believed patentable over Volfson for at least this reason.

Claim 14 recites "the dielectric coating applied to the etching exposed surfaces results in a surface substantially parallel to the wafer substrate, the coated photoresist extending substantially perpendicularly to the wafer substrate, such that the low angle of ion etching relative to the wafer substrate is a high angle relative to the extending coated photoresist." Again, Volfson does not teach coated photoresist, and certainly not coated photoresist extending perpendicularly (or in any other orientation) to the wafer substrate. Nor does Volfson recite low-angle ion etching relative to the wafer substrate.

Claim 15 requires that the via contact exposed by ion etching be in substantially the same plane as the surface substantially parallel to the wafer substrate. As noted with respect to claim 9, Volfson does not teach that via contacts are exposed by ion etching, and so

cannot teach a thus-exposed via contact that is in substantially the same plane as the surface substantially parallel to the wafer substrate.

Claims 17 and 18 recite that "ion etching is accomplished by a physically assisted process," and "the physically assisted process is reactive ion etching," respectively. As noted above, Volfson teaches neither a physically assisted ion etching (claim 17) nor reactive ion etching (18) ***performed at a low angle*** (claim 12).

Claim 22 further recites:

> depositing an additional patterned layer upon the exposed at least one via contact;
>
> depositing an additional photoresist on the additional patterned layer;
>
> masking the additional photoresist to provide at least one protected area, the additional photoresist being developed to remove the additional photoresist from the non-protected area;
>
> depositing an additional dielectric coating upon the additional patterned layer and the remaining additional photoresist; and
>
> ion etching at a low angle relative to the additional patterned layer to remove the dielectric coated additional photoresist, the removal of the additional photoresist thereby providing at least one self-aligned via contact to the additional patterned layer.

Again, Volfson fails to anticipate claim 22 at least because Volfson does not teach or suggest depositing a dielectric upon a photoresist, or etching to remove a dielectric coated photoresist, as in claim 22.

Claim 23 depends from claim 12 thorough claim 22, and thus benefits from the arguments presented herein above. In short, through its dependence on the aforementioned claims, claim 23 includes the limitations of *two* operations for depositing a dielectric upon a photo resist, and *two* operations of ion etching at a low angle to remove a dielectric coated photoresist.

Reconsideration of claims 13-15, 17, 18, 22 and 23 is respectfully requested.

**Claim 24:**

Claim 24 recites a directional ion etching process for patterning self-aligned via contacts, stated to include:

> depositing a first conductive layer on a wafer substrate;
>
> depositing a first photoresist layer on the first conductive layer;
>
> masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows;
>
> depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows;

depositing a junction layer upon the planarized dielectric, the junction layer being in electrical contact with the conductive rows;

depositing a second photoresist upon the junction layer;

masking the second photoresist to provide a plurality of junction stacks, the second photoresist being developed and the exposed junction layer being etched;

depositing a second dielectric to coat the etching exposed surfaces and the second photoresist; and

ion etching at a low angle relative to the wafer substrate to remove the dielectric coated second photoresist, the removal of the second photoresist thereby providing at least one self-aligned via contact.

As summarized above, Volfson fails to teach a process of directional ion etching , wherein the ion bean is at a low angle to the lane of the wafer, and that the low angle ion beam is used to removed dielectric coated photoresists as to form one or more self-aligned via contacts. Volfson therefore fails to anticipate claim 24 as set forth by applicant.

Reconsideration of claim 24 is respectfully requested.

**Claims 26, 27, 30-33, 35, 37 and 38:**

Claims 26, 27, 30-33, 35, 37 and 38 depend from claim 24 and benefit from like argument. As such, applicant includes herein by reference each and every statement made with respect to claim 24, above. In addition, these claims are patentable over Volfson for additional reasons, including the following:

Claim 26 recites the same limitation found in claims 2 and 17. Claim 27 recites the same limitations as claims 3 and 18. Applicant thus incorporates herein by reference the statements made above with respect to claims 2, 3, 17 and 18.

Claim 30 requires that the first dielectric is planarized by CMP planarization. Respectfully Examiner is in error – Volfson col. 4, lines 40-51 make no mention of planarization. However, Col. 6 lines 22-24 state, "The dielectric preferably is a planarizing layer such as a polymide, which is spun and cured to form a layer about 20-25 microns thick." This is fundamentally different from applicant's process of depositing the dielectric and then ***planarizing the layer*** to provide electrical connectivity to the tops of the conductive rows.

Claim 31 recites the same limitation as claim 14, only with respect to the *second* dielectric coating and the coated *second* photoresist. As noted with respect to claim 14, Volfson does not teach a coated photoresist, let alone a coated photoresist extending perpendicularly to the wafer substrate. Volfson also fails to recite low-angle ion etching relative to the wafer substrate.

Claim 32 recites "the thickness of the second dielectric coating is substantially the height of the junction stacks, such that the top surface of the dielectric coating is in substantially the same plane as the top of the junction stacks." The Examiner states that

Volfson discloses this limitation, pointing to Figure H. Respectfully, Figure H depicts two sets of copper vias 222, 236, ***not*** junction stacks, respectively surrounded by polyimide coats 216, 240.

Claim 33 recites the same limitation as claim 15. As such, applicant incorporates herein by reference each statement made in support of claim 15.

Claim 35 additionally includes:

> depositing a second conductive layer upon the exposed via contacts;
>
> depositing a third photoresist layer on the second conductive layer; and
>
> masking the third photoresist layer to provide conductive columns transverse to the conductive rows, the third photoresist being developed, the exposed second conductive layer being etched and the remaining third photoresist being dissolved to expose the conductive columns.

As previously noted, Volfson fails to teach at least two elements of claim 24. The additions of claim 35 are thus part of a process that is different from the process of Volfson. For example, claim 35 requires that a second conductive layer be deposited upon the exposed via contacts created by ion etching at a low angle relative to the wafer substrate in claim 24. Claim 35 is therefore patentable over Volfson for at least this reason.

Claims 37 and 38 recite the same limitations found in claims 22 and 23, respectively, and are patentable over Volfson for at least the same reasons. All statements presented in support of claims 22 and 23 are thus incorporated herein by reference.

Reconsideration of claims 26, 27. 30-33, 35, 37 and 38 is respectfully requested.

## CLAIM REJECTIONS – 35 U.S.C. § 103

Claims 2, 5, 16, 19-21, 25, 28, 29, 34 and 36 stand rejected under 35 U.S.C. §103(a) as being obvious over Volfson in view of U.S. Patent Number 6,391,658 granted to Gates et al. (Hereinafter, "Gates"). Respectfully we disagree.

It is thus respectfully noted that, to substantiate a *prima facie* case of obviousness, the initial burden rests with the Examiner who must fulfill three requirements. More specifically:

> To establish a *prima facie* case of obviousness, three basic criteria must be met.
>
> **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.
>
> **Second**, there must be a reasonable expectation of success.
>
> **Finally**, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The ***teaching or suggestion*** to make the claimed combination **and** the ***reasonable expectation of success*** **must** ***both be found in the prior art,*** **and not** ***based on applicant's***

***disclosure***. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

As illustrated above and contrary to the Examiner's assertion, Volfson does not teach or suggest applicant's method. Gates also fails to disclose or suggest 1) a process for depositing a dielectric upon a photoresist layer that has been used to etch a junction stack and the etched edges of the junction stack, or 2) of a process for directional ion etching.

Neither Volfson nor Gates teaches or suggests a directional ion milling process, wherein the ion beam is at a low angle (e.g., substantially parallel) to the plane of the wafer, for removing the dielectric coated photoresist to form one or more self-aligned via contacts. Thus, even when combined, Volfson and Gates cannot teach or suggest each and every limitation of claims 2, 5, 16, 19-21, 25, 28, 29, 34 and 36, as explained in further detail, below.

**Claims 2 and 5:**

Applicant notes that claim 1 is not rejected under 35 U.S.C. 103(a); however, its dependent claims 2 and 5 are rejected under this statute. Applicant agrees that the combined references do not teach each and every limitation of claim 1. Speficically, neither discloses depositing a dielectric coating upon the patterned layer and the remaining photoresist, nor ***ion etching at a low angle*** relative to the patterned layer to remove the dielectric coated photoresist. It is the removal of the photoresist that provides the advantageous at least one self-aligned via contact – an ability not found in either reference.

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071.5 USPQ2d 1596 (Fed. Cir. 1988). Respectfully, applicant notes that claims 2 and 5 inherit the limitations of claim 1. If claim 1 is patentable over Volfson in view of Gates, then claims 2 and 5 are also patentable over the combined references. Additional reasons for patentability of claims 2 and 5 over the combined references include the following:

Claim 2 requires that ion etching be accomplished by a physical ion etching – the narrowing of a claim limitation in claim 1, which in claim 1 is non-obvious. The Examiner notes that Volfson does not disclose this limitation, but states that Gates's "ion beam etching" does disclose physical ion etching. Respectfully, applicant utilizes physical ion etching at a low angle to remove a dielectric coated photoresist. The method of operation and the purpose of the operation are entirely different from Gates. Thus, the identical limitation is not taught by the combined references.

Claim 5 requires that the patterned layer be a magnetic tunnel junction layer. The Examiner recognizes that Volfson does not teach a magnetic tunnel junction. Gates does mention a magnetic tunnel junction; however, Gates's magnetic tunnel junction mesas are not created through a directional ion etching process including applicant's manner of providing self-aligned via contacts. Gates specifies that "the entire MTJ stack and the Si layers are to

be patterned using a single lithographic mask step, but using different RIE etch chemistries and the thin magnetic layers may be etched using ion beam etching" (col. 8, lines 18-21).

Respectfully, neither Volfson nor Gates teach ion etching *at a low relative angle* (claim 1). *Prima facie* obviousness has not been established and claims 2 and 5 are allowable over the teachings of Volfson in view of Gates whether considered separately or in combination.

**Claims 16 and 19-21:**

The Examiner does not issue a §103 rejection against claim 12, yet rejects claims 16 and 19-21, which depend from claim 12. Applicant agrees that Volfson in view of Gates does not render claim 12 *prima facie* obvious; for example, the references, alone or in any combination, fail to teach or suggest depositing a dielectric coating upon the etching exposed surfaces of junction stacks and the photoresist. The combined references also fail to teach *ion etching at a low angle* relative to the wafer substrate to remove the dielectric coated photoresist to provide at least one self aligned via contact.

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071.5 USPQ2d 1596 (Fed. Cir. 1988). Respectfully, applicant notes that claims 16 and 19-21 inherit the limitations of claim 12. If claim 12 is patentable over Volfson in view of Gates, then claims 16 and 19-21 are also patentable over the combined references. Additional reasons for patentability of claims 16 and 19-21 over the combined references include the following:

Claim 16 requires that the ion etching be accomplished by a physical ion etching. Claim 16 parallels claim 2 discussed above and therefore benefits from parallel argument. Likewise, claim 19 parallels claim 5 discussed above and therefore benefits from parallel argument. The arguments presented in support of claims 2 and 5 are incorporated herein by reference.

Claim 20 requires that the junction stack comprise a ferromagnetic data layer characterized by an alterable orientation of magnetization, an intermediate layer in contact with the data layer, and a ferromagnetic reference layer in contact with the intermediate layer, opposite from the data layer. Volfson does not describe *any* of these layers. Gates describes "a seed layer of 5 nm thick Py is to act as a template layer, under a 10nm antiferromagnetic layer 10nm under a ferromagnetic "fixed" layer of 10nm thick Py of iron manganese alloy"(col. 7, lines 50-53). However, Gates does not disclose or suggest ion etching at a low relative angle, nor depositing a dielectric layer onto the photoresist, and then removing it, using the ion etching at a low relative angle, to produce self-aligned via contacts. Since the photoresist is used to form the via layers, it cannot be removed after formation of the junction stacks without departing from the scope of applicant's invention. Gates discloses "The top surface of

this structure is planarized by CMP down to contact layer 34" (col. 8, lines 29-30). Thus, Gates clearly discloses a different process for forming via contacts.

Claim 21 requires that the self-aligned contacts occur on magnetic memory for use in probe based memory storage systems. Volfson is silent as to magnetic memory and to memory storage systems. Gates nowhere mentions probe-based memory storage systems.

Respectfully, *prima facie* obviousness has not been established and claims 16 and 19-21 are allowable over the teachings of Volfson in view of Gates whether considered separately or in combination.

**Claims 25, 28, 29, 34 and 36:**

Claims 25, 28, 29, 34 and 36 also stand rejected under 35 U.S.C. §103(a); however, base claim 24 is not rejected under this statute. Applicant agrees that the combined references do not render claim 24 *prima facie* obvious; for example, Volfson does not teach or suggest depositing a dielectric to coat a photoresist, or ion etching at an angle to remove a dielectric coated photoresist (see arguments in support of claim 24, above, incorporated herein by reference in their entirety). Gates also fails to teach these limitations; thus, the combined references cannot teach each and every limitation of claim 24, and so fail under 35 U.S.C. §103(a).

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071.5 USPQ2d 1596 (Fed. Cir. 1988). Hence, claims 25, 28, 29, 34 and 36 are also patentable over the combined references, at least because they depend from claim 24. Additional reasons for patentability of claims 25, 28, 29, 34 and 36 include the following:

Claim 25 recites the same limitation as claim 16, which is shown to be nonobvious herein above. The preceding argument in support of claim 16 is thus incorporated herein, by reference. Claim 28 recites the limitation found in claim 19. Claim 29 recites the same limitations as claim 20. Claim 34 requires the same limitation required in claim 21. All of these limitations are defended herein above. As such, applicant incorporates herein by reference all statements made in support of claims 19-21, and submits that claims 28, 29 and 34 are patentable over the combined references for like reasons.

Claim 36 recites "the self-aligned contacts occur on magnetic memory for use in cross-point magnetic memory array applications." As noted with respect to claim 21, and as the Examiner notes, Volfson is silent as to magnetic memory and memory storage systems. Gates nowhere mentions cross-point magnetic memory array applications.

Respectfully, *prima facie* obvious has not been established and claims 25, 28, 29, 34 and 36 are allowable over the teachings of Volfson in view of Gates whether considered separately or in combination.

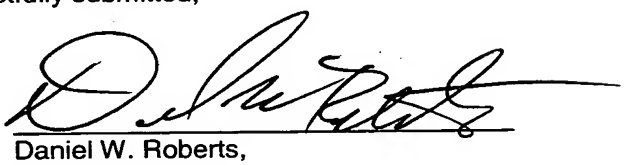
## CONCLUSION

In view of the above Remarks and the amendment to the Specification, applicant has addressed all issues raised in the Office Action dated 23 March 2005, and respectfully solicits a Notice of Allowance for claims 1-38. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant believes that no fees are due; however, should any fee be deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge deposit account 08-2025, referencing the Attorney Docket Number 200300153-1.

Respectfully submitted,

By: 

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